DAQ Training for Silicon

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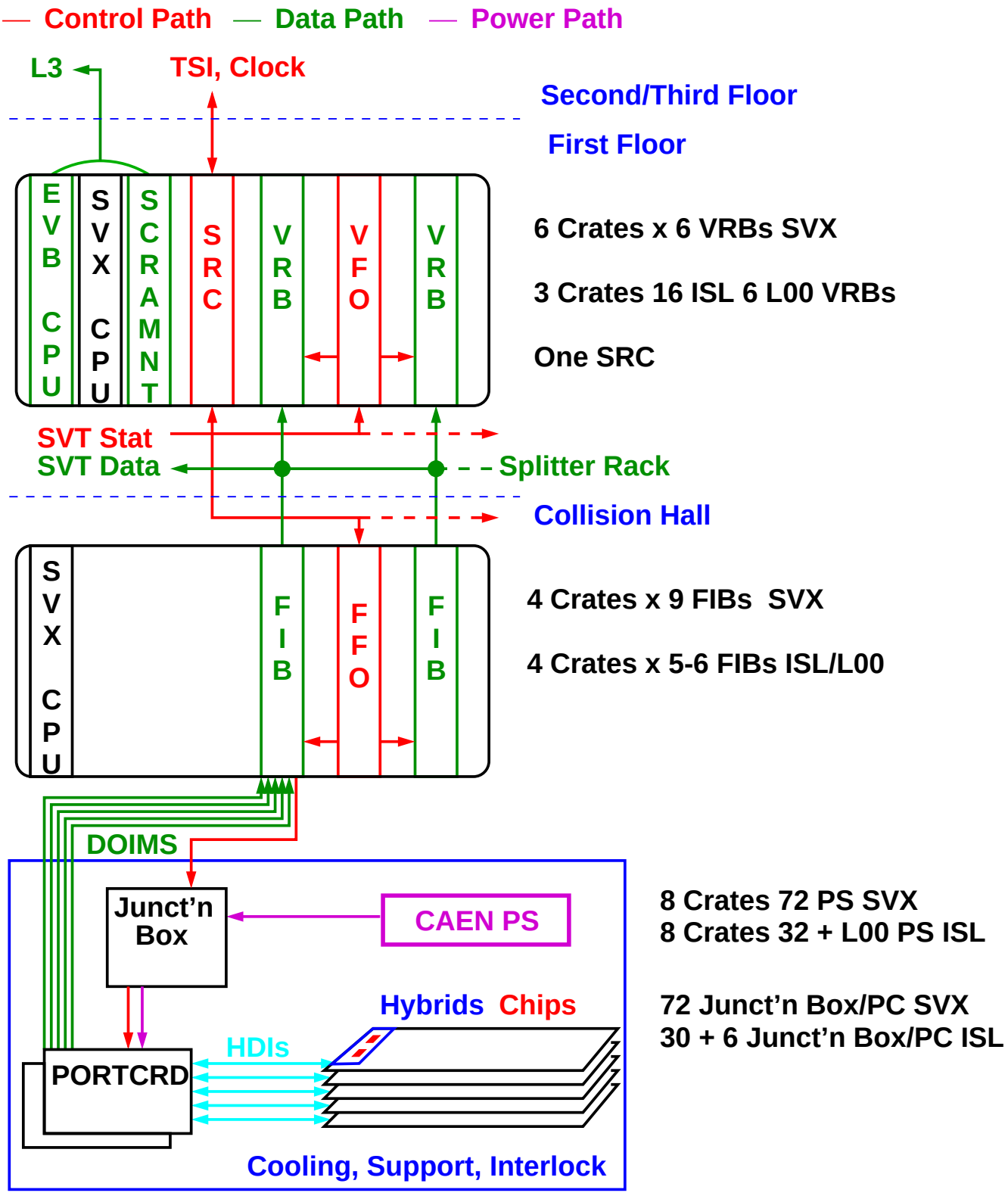
Today

Purpose:To readout the 712 kChan Silicon detector. (For this talk, there is no difference between L00, SVXII, and ISL)
Emphasis on differences from *“Normal”* DAQ

Friendly Advice:

- Learning about how things work will save time and earn **Glory and Praise**

- Your SciCo is *NOT* an expert. Don’t let them waste too much time theorizing, call a real expert.


— Control Path — Data Path — Power Path
L3
TSI, Clock
Second/Third Floor
First Floor
EVB CPU
SVX CPU
SCRAMNT
SRC
VRB
VFO
VRB
6 Crates x 6 VRBs SVX
3 Crates 16 ISL 6 L00 VRBs
One SRC
SVT Stat
SVT Data
Splitter Rack
Collision Hall
SVX CPU
FIB
FFO
FIB
4 Crates x 9 FIBs SVX
4 Crates x 5-6 FIBs ISL/L00
DOIMS
Junct'n Box
CAEN PS
Hybrids Chips
HDIs
PORTCRD
8 Crates 72 PS SVX
8 Crates 32 + L00 PS ISL
72 Junct'n Box/PC SVX
30 + 6 Junct'n Box/PC ISL
Cooling, Support, Interlock

What is Silicon DAQ: VME components

- 17 Crates: 9 Vrb crates `b0svx00-08`, 8 Fib crates `b0fib00-07` , One (SRC) `b0svx02` connected to TSI

- SRC fans out **all** trigger decisions, fans in **all** status conditions- TSI timeouts and errors **only** come from SRC (`b0svx02`) even though problems may be elsewhere.

- MVME controller only does initialization, monitoring, and X Mode calibration analysis - Readout taken care of entirely by hardware (and EVB after L2A).

- Vrbs are integral part of front end, involved in L1 processing, and are used with *BOTH* Hardware and Software EVB

What is Silicon DAQ: Non-VME components

- ~ 6000 chips spread over 557 HDIs (aka “ChipChains”), 115 PCs
  - n chips/HDI init’d by $(197 \times n$ bit) bitstream sent via Fib
  - 46 deep pipelines (42 crossings + 4 L2 buffers): `L1DONE` $\Rightarrow$ freed buffer signal SRC $\rightarrow$ TSI
- 115 Power supplies in 16 CAEN crates controlled by one VME crate.
  - All accessed by IFIX via the PS GUI
  - “Power up” conditions (currently) = `EXPERT && COOLING && BEAM OK` Changing as we get experience

- Other
  - Cooling and Interlocks controlled by IFIX
  - Radiation Monitoring System tied in with ACnet, feeds back to MCR
  - RASNIK & Inchworm alignment systems controlled by stand alone systems, logged by IFIX

Software Tasks for Silicon

- Run Control
  - Initialization: Download VME and chip parameters from HDWDB, RUNDB (`SvxSet`), pedestals and thresholds from CalibDB (`DBBroker`)
    - Chip Initialization Error

      `(MLE) b0fib00:Messenger:8:09:30 AM->Error`

      `Initializing HDI Slot 15 Chan 1:  SVX B1Wa`

      Action: Check Power, Try Again

    - VRB wacked out

      `(MLE) b0svx00:Messenger:6:03:23 AM->VRB`

      `Module ID != 3 Slot 18`

      Action: Reset that VRB (Do not power cycle crate, clean up EVB, etc).
  - Monitoring

* VME parameters and Occupancy published at 0.01 Hz. GUI soon ready for prime time.

* No CPU $\Rightarrow$ No Event Counting $\Rightarrow$ End of Run Summary show:

```
(EOR) b0fib00:  triggered 0/readout 0/sent
0 events
```

* Board error/status bits published on HALT for error diagnostics

```
(MLE) b0svx07:Messenger:7:34:19 AM->Silicon
Timeout:!DONE- Slots:  16:f420
(MLE) b0svx01:Messenger:5:32:23 PM->Silicon
Timeout:BUSY- Slots:  20:e1a0 18:e180
```

– Calibration: Several Run Types (Pedestals, Threshold and Gain Scans) being developed in both X and D Mode to calibrate the detector in the RC framework.

- SVXMon, SiliMon consumers (LBL, Liverpool)- Exhaustive online consumers makes Pulseheight spectra, Occupancy histos, monitors for data format errors, etc.

- PS GUI for PS control ($\Rightarrow$ IFIX)

- CDFVME software for Expert Diagnostics

Errors and what they mean

- General
  - TSI Timeouts (BUSY or DONE TO) *always* from SRC (`b0svx02`) though problem may be elsewhere.
  - `HALT` $\Rightarrow$ all boards queried and status published (VME GUI, Error Handler)
  - 1^{st} line of defense $\Rightarrow$ `HALT-RECOVER-RUN`
  - The **ONLY** time to reboot a `fib` or `vrb` crate is when it does not respond to a RC transition N.B. Failed Chip Initializations can take a long time
- `DONE` TO- Data did not flow from chip through Fib to Vrb after L1A- almost never happens, usually because a PS tripped

- BUSY TO- The EVB has stopped reading Vrbs (problem in SCPUs, the ATM, or Level 3). When EVB stops, Silicon VRBs become BUSY before the DAQ Vrbs

- ERROR TO- Some VME board told SRC to pull CDFERROR

  - Operational problem (Fifo overflow . . .)

  - Data format error (Events unsynchronized . . .)

- Reformatter Errors- Data corruption/Bad ladder $\Rightarrow$ reformatter cannot decode detector ID. If persistent, either the PS tripped or a ladder has gone south. Call expert.

- Erratic “Silicon Related” Errors
  Check configuration (ex: ACE_SVX_ONLY):

1. `SvxSet` $\neq$ **None**
2. `UseSrc` selected
3. `IgnoreBusy` deselected
4. All 9 Silicon Vrb crates included
   All Vrb crates must be included, though you may drop troublesome Fib crates.

- Power Supply and Cooling trips - Call Expert

- Consumer Reported Errors- UnSynch'd pipelines
  $\Rightarrow$ HRR

Experts tend to keep an eye on the Shift e-log, and there is a special Silicon e-log as well, where solutions and operations are discussed in more detail

Who and Where to get help from

- Generic

Si Ops Pager	218 8227
Problem report	cdf-silicon-op@fnal.gov

- Silicon Experts

Si Ops	G. Bolla, C. Hill
Si SubOps	S Nahn, L Miller, A Hocker, J Nielsen
DAQ	S Nahn
Slow Controls	A Ivanov, A Hocker, M Coca, Eva
Consumers	H. Bachacou, T. Shears
Other	Cast of few

- Web

`(/si=http://www-cdf.fnal.gov/internal/silicon/silicon_commission)`
`(/b0=http://www-cdfonline.fnal.gov/)`

Offical	`/si/daq.html`
Needs updating	`/b0/ace2help/svx/svxInfo.html`
Needs updating	`/b0/~svxii/runii/cdfaces/ace_daq.htm`

Do **NOT** hesitate to contact an expert. When in doubt, call the Si Ops Pager.